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Cold electronics development for the LBNE LAr TPC

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Abstract

The LBNE Project is developing a design for multiple 20 kiloton liquid argon (LAr) time projection chambers to be used as the far detector for the Long Baseline Neutrino Experiment. An essential component of this design is a complete electronic readout system designed to operate in LAr (at 90K). This system is being implemented as a CMOS ASIC, in 180 nm commercial technology, that will provide low-noise readout of the signals induced on the TPC wires, digitization of those signals at 2 MS/s, zero-suppression, buffering and output multiplexing to a small number of cryostat feed-throughs. A resolution better than 1000 rms electrons at 200 pF input capacitance for an input range of 300 fC is required, along with low power (<15mW/channel) and operation in LAr with a lifetime greater than 15 years. An analog-only frontend has been successfully completed and fully evaluated, and will be used in the MicroBooNE LAr TPC. A prototype of the digital section has been fabricated and is being evaluated. The results demonstrate that CMOS transistors have lower noise and much improved dc characteristics at LAr temperature. We will describe the progress to date and plans for the remaining development.

Keywords: Time projection chamber, Liquid argon TPC, Cryogenic electronics, CMOS ASIC

1. Introduction

The liquid argon TPC technology is uniquely suited to the measurements of interactions of neutrinos and other weakly interacting particles. It provides a relatively inexpensive high density (1.396 gm/cm^2) medium, charged particle tracking with high spatial and energy loss resolution, and the ability to scale

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detectors to very large masses. An essential component of a high resolution scalable design is an electronic signal processing chain that is located at the sense wires in the LAr (hence "cold electronics"). This removes any constraints on how the TPC modular units can be sized and arrayed, removes constraints on detector scalability, and enhances the reliability of the detector at any scale. Since charge sensing is done at the sense wires, there is no increase in charge noise that would occur with the capacitance of long cables connecting sense wires to electronics outside the cryostat: the resolution for sense wires deep within the cryostat is as good as for sense wires near the periphery. All signal feed-throughs can then be placed at the top of the cryostat, where they are easily installed, are always accessible, are at low hydrostatic pressure, and pose no risk of LAr leakage. If the cold electronic system includes digitization, buffering, and a high level of digital output multiplexing (with a level of redundancy to reduce single point failures to an acceptable level), there will be a large reduction in the number of feed-throughs and cable connections that must be made during installation, minimizing installation complexity, signal interconnect failures and cryostat leakage, which otherwise would grow to become dominant risks in very large systems. Perhaps the most significant benefit of local digital multiplexing is the reduction that it offers in the volume of cable (the "cable plant") inside the cryostat. Routing cables through the liquid creates inactive detector volumes, but more significantly the reduction of the cable plant in the gas ullage reduces correspondingly the introduction, by outgassing, of electronegative impurities into the LAr. Measurements indicate that in a stainless steel cryostat, the outgassing of cable in the ullage is the dominant source of impurities limiting electron drift distance [1].

Earlier LAr TPC detectors have used electronics located outside the cryostat ("warm" electronics). The largest of these was built by the ICARUS collaboration, and consists of two identical 0.3kt modules [2]. It achieves a noise performance about 3 times worse than has been demonstrated, for the same wire capacitance, by the electronics discussed here. The improvement in "cold" electronics noise performance is due both to the shorter connections to the sense wires and to the intrinsically better noise performance of CMOS electronics at cryogenic temperatures.

2. Detector Architecture

The proposed TPC detector modular units (Figure 1), for which these electronics are being developed, are contained in stainless steel lined cryostats containing 25kt of LAr, 24m in width, 16m in length and 49m in length. Two of these cryostats would be located in a single cavern at the 800 foot level of the

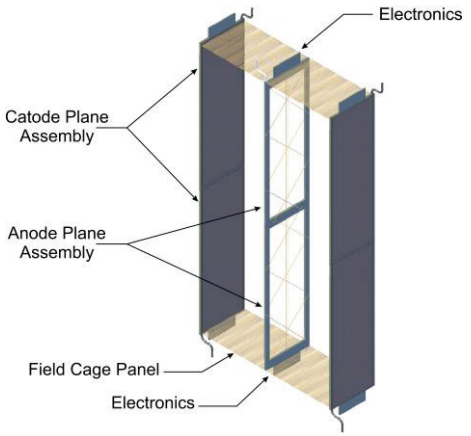
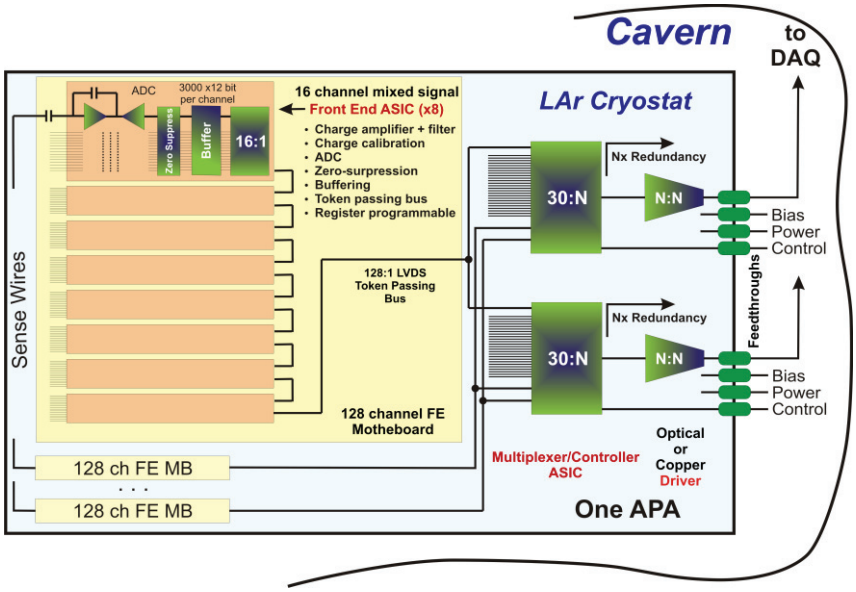


Figure 1 The modular structure of the LBNE LAr TPC. Each Anode plane assembly contains all of the readout electronics for the 2304 sense wires in the panel

former Homestake mine in Lead, South Dakota. The cryostats are foam insulated, stainless steel membrane containers commonly used to contain liquefied natural gas (LNG) in ships for transport and on land for above or below ground storage. The use of these cryostats for LAr and an overview of their construction are presented in reference [3].

Ionization electrons liberated by energetic charged particles in the LAr volume are caused to drift to arrays of sensing wires by an applied, very uniform, electric field of 500V/cm. The cathode, field cage, and anode structures for producing the uniform drift field and the sense wires for the charge signals are described in reference [4]. All of the TPC elements are designed to be modular units that can be arrayed to form detectors of any desired size. Figure 1 shows four cells of the modular structure. The anode modules are 2.5m wide by 7m tall by 7cm thick, and contain three planes of sense wires on each face, separated by the wire pitch in the drift direction. The planes are biased at voltages such that the first two planes (U & V, at ±45^{o} to the vertical) are transparent to electrons and the wires sense only induced currents, whereas the third plane (Y, vertical) is biased to collect electrons. Each wire is connected through a trace on a short printed circuit board to one channel of the electronics readout. Each unit of the

a)



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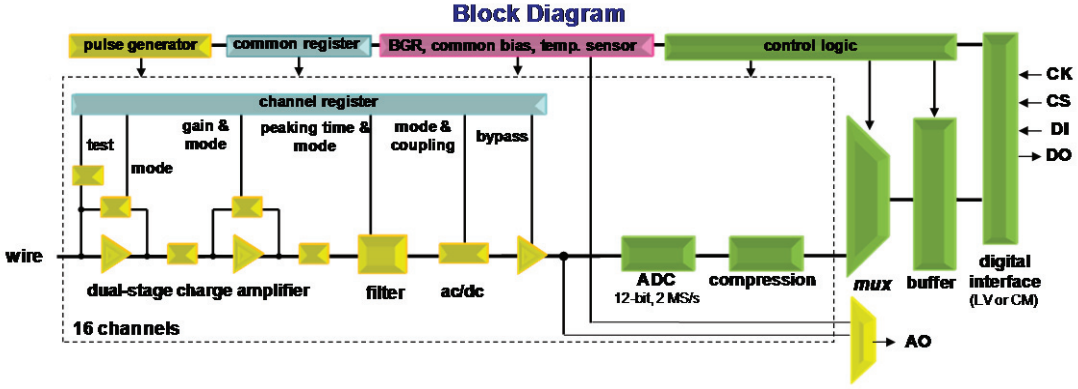

Figure 2, The modular structure of the LBNE LAr TPC. Each Anode plane assembly contains all of the readout electronics for the 2304 sense wires in the panel

TPC contains a cathode plane assembly (CPA), an anode plane assembly (APA), and a field cage segment. There are 2560 sense wires, and electronic channels, at a ~5mm pitch per APA. An entire cryostat contains 144 CPAs and 108 APAs and 354,240 channels of electronics. The detector active mass is 20kt.

The proposed architecture for the electronics readout system inside the cryostat is shown in Figure 2a, These electronics (operating in LAr at 90K) consist of front-end mixed-signal application-specific integrated circuits (ASICs) which implement the entire signal processing chain, by one (or more, for redundancy) digital multiplexing ASICs, optical or copper line drivers, and voltage regulation circuitry.

In Figure 2b, we show a block diagram of the 16-channel front-end ASIC. The ASIC includes a programmable register to control the behavior of the circuits. Each channel consists of a charge amplifier with adjustable gain, a high-order antialiasing filter with an adjustable time constant, a selectable ac/dc coupling stage, baseline adjustment to 200 mV or 900 mV for operation with either the collecting or the charge induction wires, a 12-bit 2 MSamples/s ADC, and a data compression and/or zero-suppression stage. Shared among the 16 channels are the bias circuits, registers, a temperature monitor, a pulse generator, the digital multiplexer, a channel selectable analog buffer for signal monitoring, and the digital interface. A 600 kbit buffer will be integrated in the final design, capable of storing up to 1.5 ms worth of events, sampled at 2 MSamples/s, in each channel and assuming no compression. Two or more events can be stored in a single word with compression. The projected layout size, pads included, is on the order of 11 x 6 mm^2. The expected power dissipation is below 12mW per channel with a 1.8V supply. As discussed in the next two sections, we are pursuing the final ASIC development in two separate lines: 1) the analog front-end ASIC, which has been fabricated, fully evaluated and characterized, and 2) an ADC-buffer ASIC, which has been fabricated and is being evaluated. In designing both ASICs, we have applied design rules that are expect to provide the required 15-year lifetime, as discussed in Section 5.

3. Analog front-end ASIC

The analog ASIC consists of the front-end section through the ac/dc coupling stage in Fig. 2b, including the channel programming registers and their digital interface. Details of the design of this ASIC are reported in [5]. The input MOSFET is a p-channel biased at 2 mA (3.6 mW) with a L/W ratio of 0.27μm/10mm (200 fingers, 50μm each), chosen to minimize noise, followed by a dual cascode stage [6]. At 300 K and 77 K the MOSFET offers, respectively, a transconductance of ~45 and ~90 mS and a C_g ~14pF and ~18 pF, operating at IC~0.4 and ~1.25 (i.e., in moderate inversion). The charge amplification is obtained in two stages, each with adaptive reset and nonlinear pole-zero cancellation [7], [8], and it provides a charge gain up to 20 x 16 = 320, adjustable to 4.7, 7.8, 14, and 25 mV/fC. The charge amplifier is followed by a high-order semi-Gaussian anti-aliasing filter [9] with adjustable time constant and an ac/dc coupling stage which, when enabled, introduces an ac time constant on the order of 100μs. Each channel also implements, as shown in Fig. 2b, a high-performance analog buffer capable of driving 250Ω//400pF and which, in the final version, will be replaced with a sample-and-hold stage preceding the ADC. In its current version, this analog ASIC is being used as the front end for the MicroBooNE LAr TPC detector [10]. The dissipated power is about 5mW/channel, plus an additional 5mW in each output buffer.

The ASIC integrates a band-gap reference (BGR), used to generate all of the internal bias voltages and currents (as ratios between the BGR voltage and a resistor). With the modest temperature dependence of the non-silicided resistors (a few percent from 300 K to 77 K), this bias scheme offers good stability of the operating points over a wide range of temperatures. In designing the ASIC, the operating points were set to absorb the shifts with the temperature of the MOSFET thresholds. The use of voltage feedback

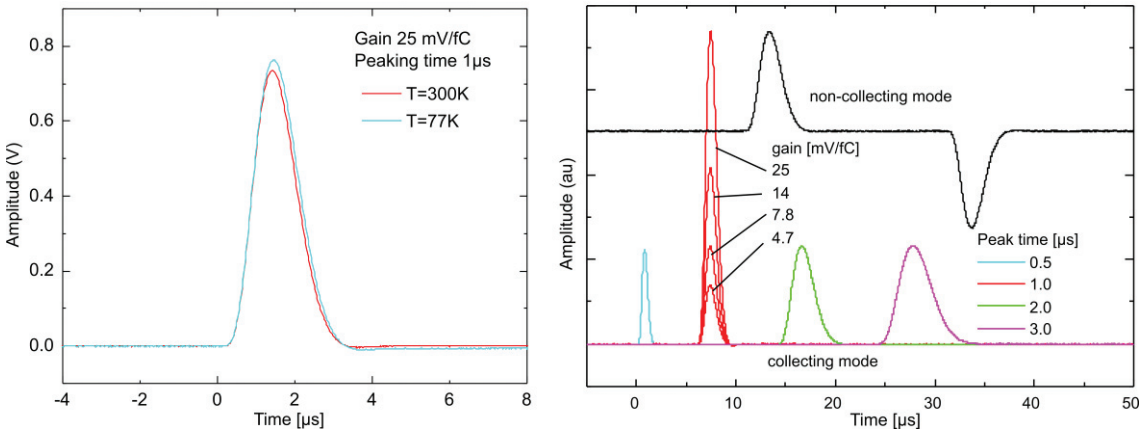

Figure 3. The front end output pulse shape at room temperature and 77K (left), and the pulse shapes for some choices of peaking time, gain, and baseline offset.

configurations with high loop gains and passive feedback components makes it possible to minimize the temperature dependence of the signal response.

The ASIC, encapsulated in a standard plastic package, was characterized both at room temperature (300 K) and fully submerged in liquid nitrogen (77 K). The text fixture was placed in a dewar which was filled with LN2 in a few seconds. During all of the tests the fixture was cycled more than 50 times between the two environments without causing any measurable changes. Figure 3 shows the measured pulse response, along with some examples of the adjustability of the gain, peaking time, and baseline offset. These results are in close agreement with the simulations and indicate that the circuits (including the digital programming interface) operate as expected in the cryogenic environment. Simulations and measurements indicate that the nonlinear pole-zero cancellation at cryogenic temperature needs to be optimized (see Figure 3, left), which will be done in the next revision of the design.

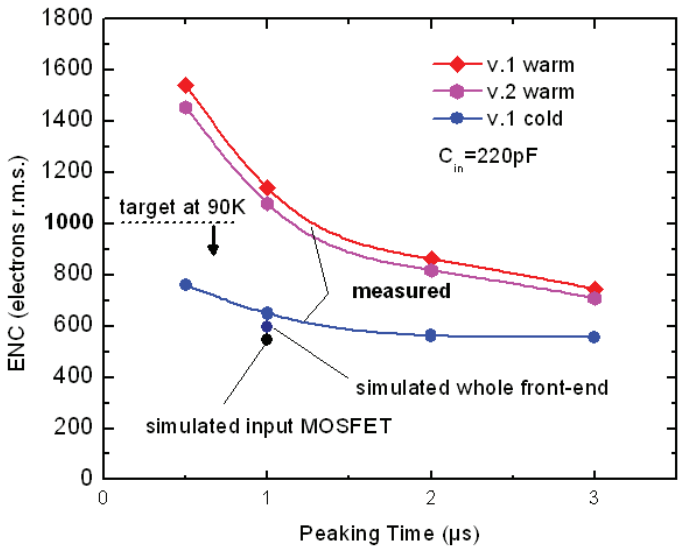

Figure 4. The equivalent noise charge for the FE ASIC as a function of peaking time at room temperature and 77K

For the purpose of charge sensitivity calibration and testing, each channel is equipped with an injection capacitor of nominal value 198 fF (size 10 x 18 μm^2) which can be enabled and disabled by a dedicated bit in the internal register. By using a precisely measured external capacitor, we extracted the value of the injection capacitance, equal to 184 fF at 300 K and 183 fF at 77 K, which is a change of less than 0.5%. This remarkable stability, along with the small change in peak shape with temperature [Fig. 3(left)], demonstrates a high stability of the passive components (resistors and capacitors). The temperature stability of the band-gap reference circuit is equally good: we measured 1.185 V at 300 K and 1.164 V at 77K, a decrease of about 1.8 %. The temperature sensor gave 867 mV at 300 K and 259.3 mV at 77K, with a response of 2.860mV/K, in close agreement with the simulations as well. The temperature independent behavior of this ASIC will be very useful for verifying the operation of assembled TPC modules before and during installation, and for verifying the operation of the entire TPC before cool-down with LAr. The measured noise will of course depend on the temperature and on the TPC filling (air or LAr) through the dielectric constant.

Fig. 4 shows the measured ENC versus the time constant (peaking time) of the entire analog chain (preamplifier, filter, buffer). At 1 μs, we measured ~650 e^-, to be compared to the simulated value of ~600 e^-. The residual difference is due to the thermal noise from the parasitic resistance of the ASIC input lines (3Ω at 77 K), which contributes to about 150 e^-. The width of those lines will be increased in the next revision in order to reduce it to negligible. A second contribution, on the order of 60 e^-, is due to the dielectric loss from the input capacitor used to simulate the wire. It is worth noting that the dielectric loss contribution will not be present with the actual sense wire.

4. ADC and Buffer ASIC

The shaped signal which results from the induction in the TPC wires must be sampled and digitized in 12-bit words at a rate of 2 MSamples/s. This is achieved by integrating one ADC in each channel. The ADC, which has been fabricated as a separate ASIC, aims to provide 12-bit resolution, converting in less than 500 ns, and dissipating about 2 mA (3.6 mW). In our design, the power can be reduced at the expense of the conversion time, which scales approximately with the inverse of the current.

The conversion occurs in two stages, the first requiring about 150 ns and providing the six most significant bits (MSBs); and the second requiring about 250 ns and providing the six least significant bits (LSBs), for a total of 12 bits resolution in about 400 ns. The remaining 100 ns are available for encoding and reset. Both stages (LSB and MSB) are based on the current mode ADC concept described in [6]. The input voltage is sampled, converted into a current, and compared with a number of matched current cells

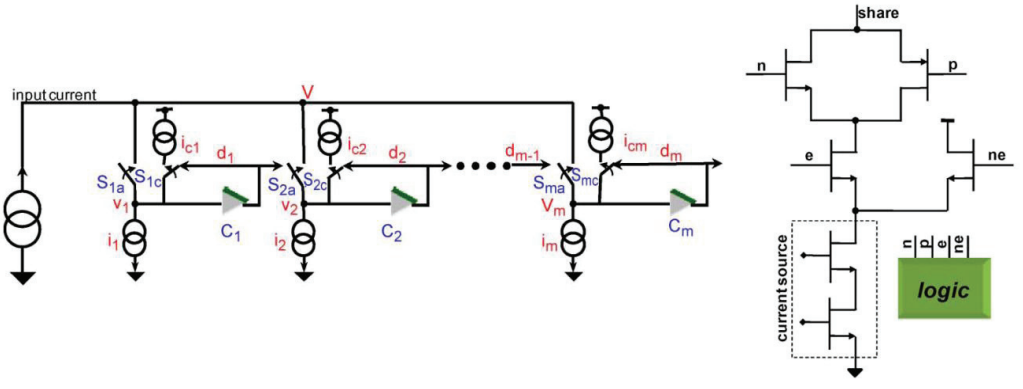

Figure 5. A simplified schematic (left), and the circuit of an individual ADC cel (right)l of the clockless ADC circuit.

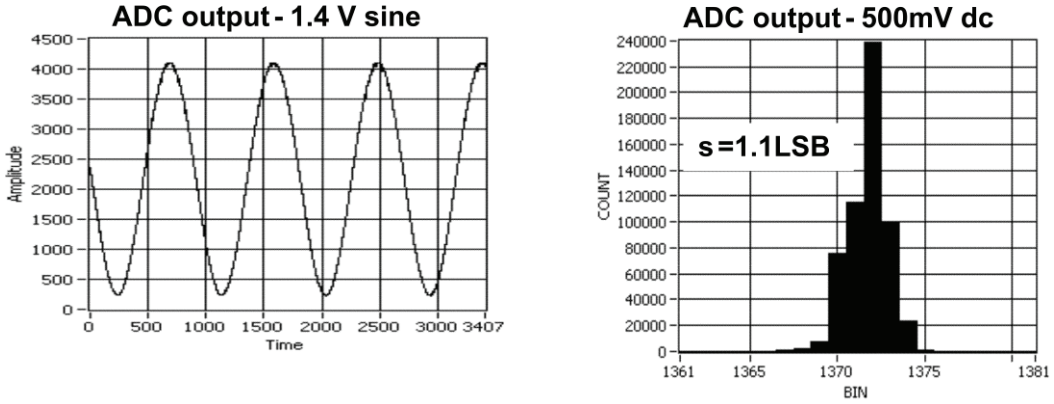

Figure 5. Preliminary results for the performance of the ADC section. For the left figure, time is in μs.

that are sequentially enabled (by the e and ne lines in the cell) to equal the input current. Fig. 5(left) shows a simplified schematic of the ADC structure. The individual cell is shown in Fig. 15(right) and it is composed of a cascoded current source, two MOSFETs controlled by signals e and ne, and providing current steering with positive feedback, two other MOSFETs controlled by signals and working as switches, and control logic. The layout size is about 1.2mm x 230 mm per channel. Details on the design and layout, along with the measured performance results, will be published as the development progresses.

5. Lifetime

To successfully design CMOS circuits that will operate at cryogenic temperatures, two critical issues must be addressed and resolved. The first is the requirement for realistic models at the operating temperature of active devices, interconnects, and passive components (resistors and capacitors) in order to reliably predict operating points, signal response, and noise during the design process. The second critical issue is the requirement that the design must ensure a long operational lifetime, since once the TPC is filled with LAr the detector must operate for about 15 years without any access to the electronics for repair or replacement. Concerning the availability of realistic models, our preliminary results from the cryogenic characterization (down to 40 K) of a complete mixed-signal ASIC [11] in a commercial CMOS 0.25μm technology, originally developed for room-temperature applications, indicates that the models are useful to first order. To refine these models, we fabricated several single-transistor test structures on each of the prototypes. Measurements of the properties of these structures at cryogenic temperatures have been used to refine the device models at 90K.

The lifetime of CMOS circuits is limited by several mechanisms which degrade the performance over time, eventually causing the circuit to fail to perform as specified. The rates of most degradation mechanisms in CMOS, such as electro-migration (EM), stress migration (SM), time-dependent dielectric breakdown (TDDB), thermal cycling (TC), and negative bias temperature instability (NBTI), all scale with temperature such that cryogenic operation is favored [12], [13]. The only mechanism that could affect the lifetime at cryogenic temperature is the degradation due to impact ionization, which causes charge trapping in the MOSFET gate oxide at large drain-current densities (the “Hot Carrier” effect). Results from [14] provide general design guidelines (for device geometry, bias, and current density) that

should guarantee a lifetime well in excess of 15 years for continuous cryogenic operation. These design guidelines also provide information for designing test conditions to observe the deterioration mechanism and to extrapolate from accelerated deterioration rates, measured under stressed conditions within practical times, to the ultimate lifetime under normal operation.

A monitor of the impact ionization is the bulk current, which reaches a maximum at $V_{DS} = V_{DD}$ and at $V_{GS} = 0.5\ V_{DD}$. When operating constantly in this condition at room temperature, a properly designed device will typically have a lifetime (defined as a 10% degradation in g_m) of about 10 years. The bulk current (i.e., the impact ionization) increases roughly a factor four from 300K to 77K [14], and a circuit designed for operation at room temperature would have a proportionately shorter useful life at cryogenic temperature. As stated above, in order to guarantee the required lifetime at cryogenic temperatures, design guidelines must be modified for both analog and digital circuits. For analog circuits, this is done by operating the devices at moderate-to-low drain current densities, where impact ionization becomes negligible. For digital circuits, operating the devices with reduced V_{DD} (about 20%) and using non-minimum channel length L, which is easily accommodated since at cryogenic temperature the speed of the digital circuit increases [15], compensating for the increased L. We will verify these guidelines with accelerated aging tests, at increasing values of V_{DD}, on dedicated structures. Such tests also will be conducted on prototype samples throughout the development process to verify the long-term reliability of the final ASICs.

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